SMFL CMOS Details

SA-CMOS Process

- RIT 2 µm Twin-well CMOS process
- LOCOS isolation
- Common boron VT adjust implant
- N+ poly gate, 300 Å gate oxide
- 2-level Aluminum metallization

Performance Parameters

- VTn = 1 V, VTp = -1 V
- Leff ~ 1.5 µm
- RDSn = 1.5 kO-µm, RDSp = 3 kW-µm
- SSn ~ 105 mV/dec, SSp ~ 90 mV/dec
- Rsn = 24 O/?sq , Rsp = 60 O/?sq
- Poly Rs = 35/80 O/?sq (nmos/pmos)

Design & Layout Specifications

- Conservative MOSIS design rules, l = 2 µm
- Poly shrink will reduce gate length to 2 µm
- Contacts & vias will remain 4 µm x 4 µm
- 1X contact print or 5X reduction lithography
- Preferred file format: gdsii

Process Options

- Custom threshold adjustments, multiple VTs
- 1.5 µm gate length option, Leff ~ 1 µm
- Dual workfunction
- Custom metallization
- 1X & 5X lithography mix & match