

# SMFL CMOS Details

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## SA-CMOS Process

- RIT 2  $\mu\text{m}$  Twin-well CMOS process
- LOCOS isolation
- Common boron VT adjust implant
- N+ poly gate, 300  $\text{\AA}$  gate oxide
- 2-level Aluminum metallization

## Performance Parameters

- $V_{Tn} = 1 \text{ V}$ ,  $V_{Tp} = -1 \text{ V}$
- $L_{eff} \sim 1.5 \mu\text{m}$
- $RDSn = 1.5 \text{ k}\Omega\text{-}\mu\text{m}$ ,  $RDSp = 3 \text{ kW-}\mu\text{m}$
- $SSn \sim 105 \text{ mV/dec}$ ,  $SSp \sim 90 \text{ mV/dec}$
- $R_{sn} = 24 \text{ O}/\mu\text{sq}$ ,  $R_{sp} = 60 \text{ O}/\mu\text{sq}$
- Poly  $R_s = 35/80 \text{ O}/\mu\text{sq}$  (nmos/pmos)

## Design & Layout Specifications

- Conservative MOSIS design rules,  $l = 2 \mu\text{m}$
- Poly shrink will reduce gate length to  $2 \mu\text{m}$
- Contacts & vias will remain  $4 \mu\text{m} \times 4 \mu\text{m}$
- 1X contact print or 5X reduction lithography
- Preferred file format: gdsii

## Process Options

- Custom threshold adjustments, multiple VTs
- 1.5  $\mu\text{m}$  gate length option,  $L_{eff} \sim 1 \mu\text{m}$
- Dual workfunction
- Custom metallization
- 1X & 5X lithography mix & match